

5 a register which stores a value which is representative of a
6 delay time after which the memory device responds to a read
7 request; and

8 a plurality of output drivers to output data in accordance
9 with the delay time and synchronously with respect to the external
10 clock signal.

2
1 152. The memory device of claim 151 further including:

2 clock generation circuitry, coupled to the clock receiver
3 circuitry, to generate at least one internal clock signal; and

4 wherein the plurality of output drivers output data in
5 response to the internal clock signal.

1 153. The memory device of claim 152 wherein the plurality of
2 output drivers output data in response to a rising edge of the
3 internal clock signal.

4
1 154. The memory device of claim 151 further including:

2 a delay locked loop, coupled to the clock receiver circuitry,
3 to generate an internal clock signal using at least the external
4 clock signal; and

5 wherein the plurality of output drivers output data in
6 response to the internal clock signal.

5
1 155. The memory device of claim 151 wherein the value which is
2 representative of the delay time is stored in the register after
3 power is applied to the device.

1 ⁶²156. The memory device of claim ¹151 wherein the value stored
2 in the register is representative of one of a plurality of
3 different delay times.

1 ¹³157. A synchronous semiconductor memory device having at least
2 one memory section including a plurality of memory cells, the
3 memory device comprising:

4 clock receiver circuitry to receive an external clock signal;
5 at least one register to store a value which is representative
6 of a delay time; and

7 wherein in response to a read request, the memory device
8 outputs data in accordance with the delay time and synchronously
9 with respect to the external clock signal.

1 ¹²158. The memory device of claim ¹¹157 further including:
2 clock generation circuitry, coupled to the clock receiver
3 circuitry, to generate an internal clock signal; and

4 an output driver, coupled to the internal clock generation
5 circuitry, to output the data in response to the internal clock
6 signal.

1 ¹³159. The memory device of claim ¹²158 wherein the output driver
2 outputs data in response to a rising edge of the internal clock
3 signal.

1 ¹⁴160. The memory device of claim ¹¹157 further including a delay
2 locked loop, coupled to the clock receiver circuitry, to generate

3 an internal clock signal using at least the external clock signal
4 and wherein the output driver outputs data in response to the
5 internal clock signal.

1 ~~161~~. The memory device of claim 157 wherein the memory device,
2 in response to a set register request, stores a value in the at
3 least one register.

1 ~~162~~. The memory device of claim ~~157~~ wherein the value stored
2 in the register is representative of one of a plurality of
3 available delay times.

1 ~~163~~. A method of operating a synchronous semiconductor memory
2 device having at least one memory section including a plurality of
3 memory cells and a register for storing a value which is
4 representative of a time delay after which the memory device
5 responds to a read request, the method comprising:

6 issuing a read request to the memory device wherein the memory
7 device, in response to the read request, outputs data on a bus in
8 accordance with the time delay and synchronously with respect to an
9 external clock signal.

1 164. The method of claim 163 further including issuing a set
2 register request, wherein, in response to the set register request,
3 the memory device stores the value in the register.

1 165. The method of claim 164 wherein the set register request
2 and the value are provided to the memory device in a single request
3 packet.

1 ²⁶166. The method of claim ²³163 wherein the read request and
2 information identifying the time delay after which the memory
3 device responds to a read request are provided to the memory device
4 in a single request packet.

1 ²⁷167. The method of claim ²⁸163 further including the steps of:
2 initializing the register in the memory device by issuing a
3 set register request on the bus; and
4 providing the value which is representative of the time delay.

1 168. The method of claim 163 further including the step of
2 identifying the memory device on the bus using a device
3 identification code.

1 ²⁹169. The method of claim ²⁸168 wherein the device identification
2 code and information identifying the time delay after which the
3 memory device responds to a read request are provided to the memory
4 device in a single request packet.

1 ³⁰170. The method of claim ²⁸168 wherein the device identification
2 code is a unique device code.